文章编号 1674-2915(2013)02-0196-05

Energy measurement of high-repetition-rate pulsed laser

FENG Gang*, FENG Guo-bin, SHAO Bi-bo, YAN Yan, WANG Zhen-bao
(*State Key Laboratory of Laser Interaction with Matter, Northwest Institute of Nuclear Technology, Xi'an* 710024, *China*)
* *Corresponding author, E-mail: fenggang*9731@*yeah.net*

Abstract: A peak value hold circuit is developed for the energy measurement of a high-repetition-rate pulsed laser. The circuit consisting of four modules including a charge integrator, a 2nd-order Butterworth low-pass filter, a time-delay trigger and a peak-value-holder is designed to convert the photocurrent pulses to voltage pulses which are linear to the energies of incident pulse laser. The experimental measurement results indicate that this circuit is suitable for the pulsed laser with a width less than 10 ns and a repetition rate over 2 kHz. The results show that the circuit has a dynamic range about 140 times and works stably. It can be used to achieve a high spatial resolution in photodiode measurement systems.

Key words: laser energy measurement; high-repetition-rate pulse laser; peak value hold circuit; charge integrator

高重复频率脉冲激光能量测量

冯 刚*,冯国斌,邵碧波,闫 燕,王振宝
(西北核技术研究所 激光与物质相互作用国家重点实验室,陕西 西安 710024)

摘要:设计了一种用于高重复频率脉冲激光能量测量的峰值保持电路。电路由电荷积分器、2阶低通滤波器、时间延迟触发器和峰值保持器组成,通过将光电流脉冲转换成电压脉冲,电压脉冲的峰值与对应电流脉冲所包含的能量成正比。实验测量结果表明:该电路可以测量脉宽<10 ns,重复频率≥2 kHz的重频窄脉冲激光的脉冲能量,且工作稳定,其线性动态范围≥140倍。该电路可应用于光电阵列探测系统中,能实现较高的空间分辨力。

关 键 词:激光能量测量;高重复频率脉冲激光;峰值保持电路;电荷积分器
中图分类号:TN247 **文献标识码**:A doi:10.3788/CO.20130602.0196

收稿日期:2012-12-21;**修订日期**:2013-02-23

1 Introduction

When the far-field density distribution of a diode pumped laser is measured, a typical method is to use the photoelectric detector array. The diode pumped laser is characterized by short pulses (about 10 ns) and high repetition rates ($\geqslant$ 2 kHz). To measure the pulsed laser, the energy of each pulse is expected to be acquired and an ultrafast Analog-to-Digital-Converter (ADC) must be used. However, when a high spatial resolution detector array is empolyed, more than three hundred detectors would be contained and using an ultrafast ADC for each channel seems impossible. So some improvements must be done on the conditional circuit. A peak value hold circuit was designed in this paper. The circuit converts current pulses to voltage pulses and then broadens the pulse width to a proper duration. Thus multiplexers and low speed ADCs could be used and a higher spatial resolution could be achieved.

Now, there are many ways to implement the peak value hold circuit[1-10], including a monolithic peak detector, PKD01, from Analog Devices, Inc[5]. Unfortunately, some of those circuits are too complicated to apply in a multi-channel system and some circuits can only receive pluses with a slow rising edge, while others were designed to record a single pulse, not for repetitive pluses. In this solution, a charge integrator is constructed to convert a current pulse to a voltage representing the energy that pulse contains, then a low-pass filter is inserted to reduce high frequencies and increase stability. Finally, a peak-value-holder following the filter will track and hold the peak value of every pulse. An output of low frequency squarewave makes signal acquisition and data processing become more flexible.

2 Circuit design

2.1 Architectural overview

The circuit is primarily made up of four modules besides a high-speed silicon photodiode, including a charge integrator, a 2nd-order Butterworth low-pass filter, a time-delay trigger and a peak-value-holder. Fig. 1 is the functional block diagram.

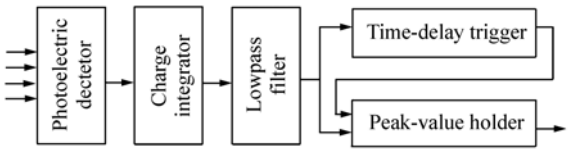


Fig. 1　Functional block diagram of the circuit

2.2 Charge integrator

A high-speed silicon photodiode with a bias of 12 V is used to convert the optical power to an electrical current. An optical pulse will be converted to an electrical current pulse with the same profile. By using the charge integrator, the electrical current pulse will be converted to a voltage proportional to the energy the pulse contains.

The charge integrator is mainly composed of an operational amplifier and an integration capacitor. The operational amplifier should offer high slew rate to deal with the short pluses. And in order to reduce the input bias current, FET inputs are necessary. When a pulse arrives, the integration capacitor is charged and the operational amplifier's output raises until the pulse ends. To measure repetitive pluses, the integration capacitor should be discharged before the next pulse arrives. A resistance is connected in parallel with the integration capacitor to simplify the circuit structure. Parameters of the capacitor and resistance should be carefully calculated. First, the amount of photocurrent should be estimated based on the optical power and the responsivity of the photodiode. Second, the value of the integration capacitor

can be calculated based on the photocurrent and the operational amplifier´s output swing. Finally, the value of the resistance should be determined according to the repetition rate and the RC time-constant. When an integrating approach ends, the integration capacitor would discharge through the resistance. So the integrator will output a series of voltage pulses with fast rising edge and exponential falling edge. The peak value of each pulse is proportional to the energy the corresponding optical pulse contains. Fig. 2 is the schematic circuit diagram of the charge integrator. A photodiode and the noise filter are also illustrated in Fig. 2.

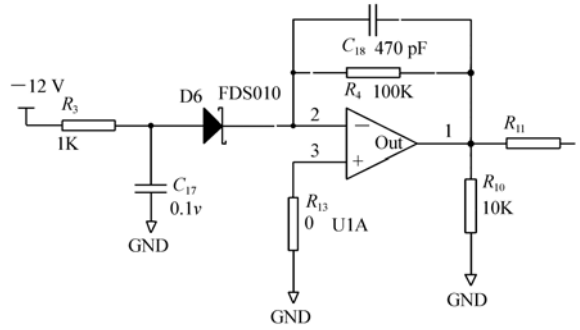


Fig. 2 Schematic circuit diagram of charge integrator

2.3 Low-pass filter

The rising edge of the integrator′s output is so fast that it may cause the circuit unstable. To resolve this problem, a low-pass filter can be inserted between the charge integrator and the peak-value-holder. A 2nd-order Butterworth low-pass filter was designed. The filter is made up of only five components, which includes an operational amplifier, two resistances and two capacitors. In order to deal with high speed analog signal, the operational amplifier must be high speed operational amplifier. For this design, the cutoff frequency was set at about 10 kHz. The cutoff frequency can be easily adjusted by modifying values of the resistances or capacitors. The filter also outputs a series of voltage pluses, but with slower rising edge.

2.4 Peak-value-holder

The filter outputs pluses with slow rising edge, which means that a compact but effective peak-value-holder could be used. Fig. 3 shows the schematic circuit diagram of a peak-value-holder.

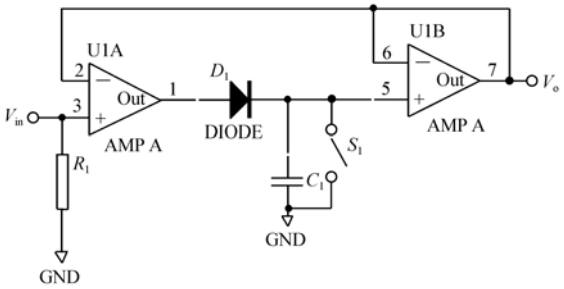


Fig. 3 Schematic circuit diagram of peak-value-holder

As shown in Fig. 3, a dual operational amplifier, a diode and a hold capacitor were used to construct a peak-value-holder, as well as an analog switch. The two amplifiers works as a voltage follower, while second one(U1B) offers the output drive capability and makes the leakage current of the capacitor(C1) much lower. When a pulse arrives, the diode(D1) is conducting on the rising edge and off on the falling edge. So the peak-value-holder will output a voltage equal to the peak value of the pulse. The analog switch(S1) is controlled by a digital signal. Just before a pulse arrives, the switch is put off when the peak-value-holder would track the input signal and hold the peak value. Some time later the switch will be put on and the output will resume to 0 V.

2.5 Time-delay trigger

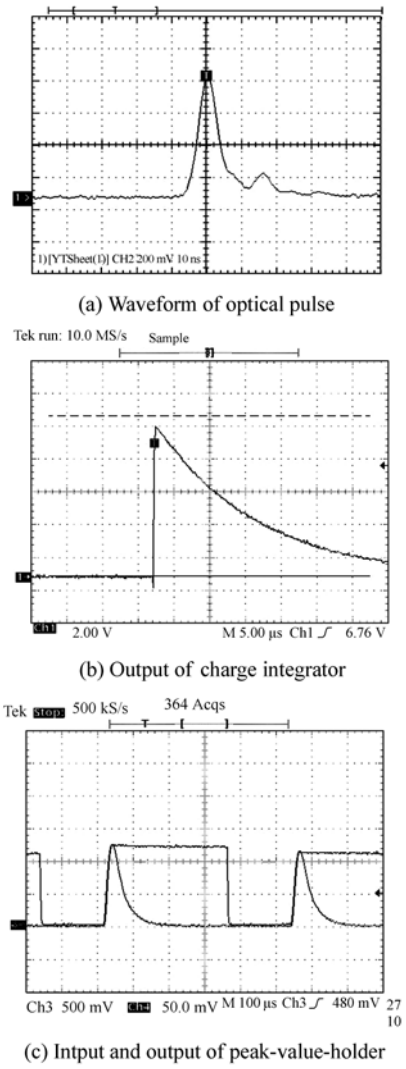
A time-delay trigger is designed to realize self-trigger, i. e. the system will trigger itself by the input pulse, but not an external signal. The unit accepts the low-pass filter′s output as its input and outputs a control signal for the analog switch. Putting on the analog switch will reset output of the peak-value-holder to 0 V, which should be accomplished before a next pulse is on the input pin.

To construct the trigger, a comparator is used to convert an analog pulse to a digital pulse. The digital pulse will be delayed for about 400 μs, which can be adjusted if necessary, and then puts on the ana-

log switch. A dual non-retriggerable monostable multivibrator is used to implement the time-delay function in the prototype design. A Complex Programmable Logical Device (CPLD) used in a multichannel to do this will be more effective and helpful. The delay time can be adjusted by modifying the design parameters, no need to change the circuit structure.

3 Testing results

The prototype circuit is tested in library under a diode pumped laser with a repetition rate of 2 kHz and pulse width of about 10 ns. Some typical waveforms are shown in Fig. 4.



(a) Waveform of optical pulse

(b) Output of charge integrator

(c) Intput and output of peak-value-holder

Fig. 4　Typical waveforms

As shown in Fig. 4, width of optical pulse is about 10 ns. The width is broadened after the integrating approach, but the rising edge is still very steep. When the Butterworth filter is applied, the high frequencies are filtered and the rising edge became smoother as shown in Fig. 4(c). Waveforms in Fig. 4(c) show that the peak-value-holder can perfectly hold the peak value of the pulse as expected. Some testing results are shown in Fig. 5, in which x-axis represents the energy of a single pulse, while the y-axis represents the voltage outputs by the peak-value-holder.

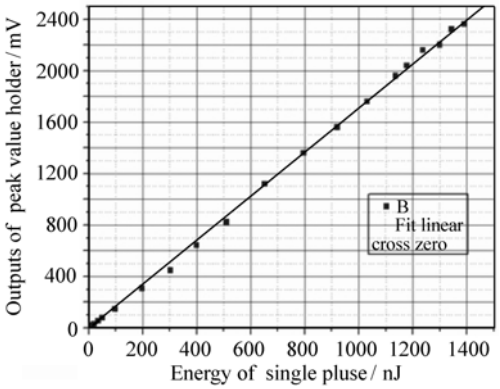


Fig. 5　Testing results

A cross-zero linear fitting curve in Fig. 5 shows excellent linearity of the circuit and the linear dynamic range is more than 140 times. Good stability can also be achieved.

4 Conclusion

A peak value hold circuit was designed for the energy measurement of a high-repetition-rate pulsed laser. The circuit can accept a series of pluses as its input and output a squarewave with adjustable duration. Thus multiplexers and low speed ADCs can be used to achieve higher spatial resolution when a detector array is empolyed. The pulses with width less than 10 ns can be measured and the measurable repetition rate is not less than 2 kHz. The whole circuit

is made up of two dual-amplifiers, a comparator, an analog switch and some passive chips. High spatial resolution, good linearity and stability can be achieved by employing this design. This design can also be applied in other fields where pulse energy measurement is needed.

References:

[1] MAXIM C. Inexpensive peak detector features droopless operation[EB/OL]. (2001-01-26)[2012-07-25]. http://www.Maxim-ic.com.cn/appnotes.cfm/an_pk/1163.

[2] JIM McL, BILL T. Precision peak detector uses no precision components[EB/OL]. (2004-06-10)[2012-07-25]. http://www.edn.com/article/CA421510.html.

[3] SHYAM TIWARI. Sampling peak detector has shutdown feature[EB/OL]. (2002-03-16)[2012-07-25]. http://www.edn.com/article/CA216167.html.

[4] ANALOG DEVICES. Inc., Monolithic peak detector with reset-and-hold mode:PKD01[EB/OL]. [2012-07-25]. http://www.analog.com/static/imported-files/data_sheets/PKD01.pdf.

[5] LIU H Y, SHI X J. The design on practical peak value detector with interrupt output[J]. *Chinese J. Electron Devices*, 2003, 26(1):104-106. (in Chinese)

[6] YI X J, YE CH SH. Design of high speed digital peak holding circuit based on FPGA[J]. *Modern Machinery*, 2005(4): 9-10. (in Chinese)

[7] LIU H B, WANG X SH, CH ZH. Design of transconductance peak holding circuit for fast narrow pulse[J]. *Optical Technique*, 2008, 34(suppl):233-235. (in Chinese)

[8] PENG Y, SU H, DONG CH F, *et al*.. A peak holding circuit for fast narrow pulse[J]. *Nuclear Electronics & Detection Technology*, 2007, 27(2):254-256. (in Chinese)

[9] LI Q, LIU SH X, NIE B M. Research on a peak holding and data acquisition circuit for nuclear pulse[J]. *J. Electronic Measurement and Instrument*, 2009(suppl):363-366. (in Chinese)

[10] ZHANG L, SHAO B B, YANG P L, *et al*.. Diagnosis of high-repetition-rate pulse laser with pyroelectric detector[J]. *Chinese Optics*, 2011, 4(4):404-410. (in Chinese)

作者简介:

冯 刚(1981—),男,湖北京山人,工程师,2004年于武汉大学获得学士学位,2007年于西北核技术研究所获硕士学位,主要从事信号与信息处理方面的工作。E-mail: fenggang9731@yeah.net

冯国斌(1971—),男,湖北黄石人,研究员,1990年于国防科技大学获得学士学位,2000年于西北核技术研究所获得硕士学位,主要从事激光参数测量及激光与物质相互作用方面的研究。E-mail:fgb02@163.com

邵碧波(1962—),女,浙江杭州人,高级实验师,1986年于国防科技大学获得学士学位,主要从事激光参数测量方面的工作。E-amil: shao_bb@126.com

闫 燕(1979—),女,陕西子长人,工程师,2003年于四川大学获得学士学位,主要从事激光参数测量方面的工作。E-mail:78385578@qq.com

王振宝(1981—),男,内蒙古呼伦贝尔人,硕士,助理研究员,2002年于四川大学获学士学位,2004年于国防科技大学获硕士学位,主要从事激光技术及应用方面的研究。E-mail:zhenbao_wang98@163.com