文章编号 2095-1531(2019)05-1076-14

Study on the photo response of a CMOS sensor integrated with PIN photodiodes

YANG Cheng-cai[1,2], JU Guo-hao[1,2,3], CHEN Yong-ping[1*]
(1. *Key Laboratory of Infrared Imaging Materials and Detectors, Shanghai Institute of Technical Physics, Chinese Academy of Sciences, Shanghai* 200083, *China*;
2. *University of Chinese Academy of Sciences, Beijing* 100049, *China*;
3. *School of Information Science & Technology, Shanghai Tech University, Shanghai* 201210, *China*)
* *Corresponding Author, E-mail: chen_yp@mail.sitp.ac.cn*

Abstract: Traditional CMOS image sensors generally use PN photodiodes or PPDs as the photosensitive element, which are formed based on N-well/P-type substrates using the LV-CMOS process. The PIN photosensitive element has small junction capacitance and high quantum efficiency. By using High-Voltage CMOS(HV-CMOS), monolithic integration of CMOS circuits with PIN photodiodes can be achieved. In this paper, the relationship between the photo-response characteristics, NEP of CMOS detectors and pixel size and reset voltage are studied. The results show that the pixel charge gain can be increased by about one order of magnitude when the photosensitive element is changed from PN to PIN and the transient charge gain of the pixel is larger than $1/C_{pd}$. This is closely related to the size of the diode and reset voltage. It is found that small pixels are more suitable for fast detection of short integration time under weak signals because of their higher charge gain and lower equivalent noise. If combined with microlenses, small pixels can be further advantageous in low light detection.

Key words: CMOS image sensor; HV-CMOS; PIN photodiodes; 3T pixel structure

集成 PIN 光敏元的 CMOS 探测器光电响应特性研究

杨成财[1,2], 鞠国豪[1,2,3], 陈永平[1*]
(1. 中国科学院 上海技术物理研究所 红外成像材料与器件重点实验室, 上海 200083;
2. 中国科学院大学, 北京 100049;
3. 上海科技大学 信息科学与技术学院, 上海 201210)

摘要: 传统的 CMOS 图像传感器一般采用基于 LV-CMOS 工艺的 N 阱/P 型衬底制备的 PN 光电二极管或者 PPD 二极管作为光敏元。PIN 光敏元具有结电容小、量子效率高的特点。采用 HV-CMOS(高压 CMOS)工艺可以实现 CMOS 电路与 PIN 光敏元的单片集成。本文研究了集成 PIN 光敏元的 CMOS 探测器的光电响应特性以及 NEP 随像素大小和复位电压的变化关系。研究表明, 将光敏元从 PN 光电二极管改为 PIN 光电二极管后, 像素电荷增益可以提高一个数量级左右; 同时, 像素的瞬态电荷增益要大于传统认为的 $1/C_{pd}$, 并与二极管的大小以及复位电压紧密相关。研究发现, 小像素因其更

收稿日期: 2018-11-07; **修订日期**: 2018-12-29

高的电荷增益和更低的等效噪声,更加适合弱信号下的短积分时间快速探测。若配合微透镜的使用,小像素在微光探测方面可以获得更大的优势。

关　键　词:CMOS 图像传感器;HV-CMOS;PIN 光电二极管;3T 像素结构
中图分类号:TN2; O472 + .8　　**文献标识码**:A　　doi:10.3788/CO.20191205.1076

1 Introduction

Low light level imaging is an optical imaging process under conditions with low illumination (below 10^{-2} lx). It plays an important role in aerospace, meteorological observation and military reconnaissance[1-4]. With the development of CMOS technology, CMOS image sensors began to replace CCDs and gradually extended to the field of low-light-level imaging[5-7]. At present, the most commonly used CMOS image sensor generally uses 3T or 4T pixel structures with photodiodes based on PN type due to the limitation of CMOS process compatibility. 4T pixels can achieve higher sensitivity and lower noise due to the addition of a charge transfer transistor and readout floating capacitors, but it also limits the size of pixels and are not suitable for the development of large pixel devices. The PIN photodiode is a special form of PN photodiode. It has the advantages of small junction capacitance, fast response speed, high quantum efficiency and no absolute restriction on pixel size[8]. However, the fabrication of PIN photosensitive elements is not compatible with the standard low voltage CMOS process (LV-CMOS). At present, most of the research on the integration of PIN photosensitive elements and CMOS circuits is based on SOI process[9-10].

In this paper, the photo-response characteristics of CMOS image sensors with a PIN photodiode as the photosensitive element in HV-CMOS processes are analyzed, with special attention given to the effects of pixel size and reset voltage on the photo-response characteristics and the noise equivalent power (NEP) of the detector.

2 HV-CMOS process

Compared with the standard LV-CMOS process, the HV-CMOS process (shown in Fig. 1) adds a lightly doped p-type epitaxial layer with a thickness of about 20 μm and a resistivity of 400 ~ 1 000 Ω · cm to the heavily doped p-type substrate. At the same time, in order to meet the low resistivity requirement (1 ~ 10 Ω · cm) of the substrate of CMOS circuits, deep N-wells were fabricated on the p-type epitaxial layer in the MOS region before the fabrication of the PMOS and NMOS. Then the CMOS circuit was fabricated on the deep N-wells using the standard LV-CMOS process, while photosensitive elements were fabricated directly on the high-resistivity p-type epitaxial layer. In this way, monolithic integration of a PIN photosensitive element and a CMOS circuit was formed (shown in Fig. 2)[11].

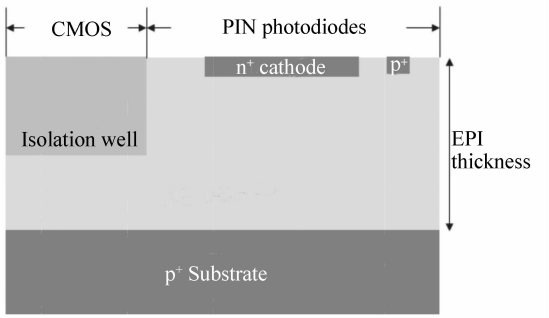

Fig. 1　Schematic diagram of HV-CMOS process
图 1　HV-CMOS 工艺示意图

CMOS circuits fabricated through this process can operate at high voltages. Now, this process is one of the standard CMOS fabrication processes.

In this process, PIN photodiodes consist of a heavily doped p(p +) region (P layer), a lightly doped p(p −) epitaxial layer(I layer) and a heavily doped n(n +) region(N layer). The existence of the intrinsic layer(I layer) increases the width of the depletion region and quantum efficiency of the diode, which is the fundamental reason that the sensitivity of PIN photodiode is higher than that of the PN

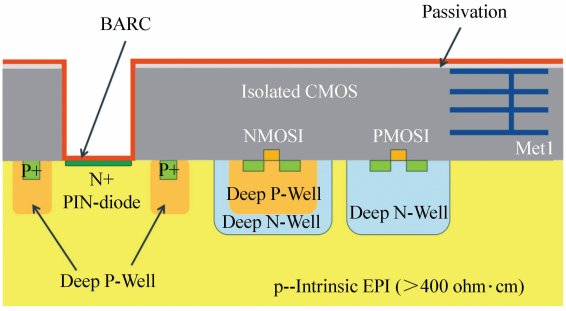

Fig. 2 Monolithic integration of PIN photosensitive element and CMOS circuit

图 2 PIN 光敏元与 CMOS 电路单片集成

photodiode. On the other hand, the thick dielectric layer formed on the surface of PIN photosensitive element can be removed in this process and the quantum efficiency of the photosensitive element can be further improved by replacing it with a single layer of antireflection coating.

3 3T pixel structure

The CMOS sensor with a PIN junction as the photosensitive element can use a 3T pixel structure (shown in Fig. 3). This structure is advantageous for its simple structure and high filling factor[12]. In the pixel structure, the PIN photodiode is the only photosensitive part of the whole CMOS image sensor; M1 is a reset transistor, through which the photodiode is reset to the reverse bias voltage value when the signal is read out; and M2 is a follower transistor, responsible for the pixel signal readout. In order to reduce the effect of charge injection, the size of the reset transistor should be as small as possible.

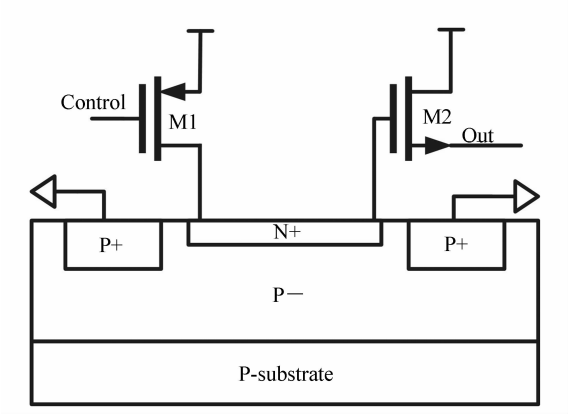

Fig. 3 3T pixel structure in HV-CMOS process

图 3 HV-CMOS 工艺中的 3T 像素结构

Compared with the 3T pixel structure, the 4T pixel adds a charge transfer tube and a floating capacitor which needs a special design behind the photodiode for it to achieve true correlation double sampling. However, this also makes the 4T pixel production process complex and costly. Furthermore, in order to achieve higher sensitivity, the capacitance of the floating capacitor is smaller, which makes it inconducive to the development of large-pixel devices.

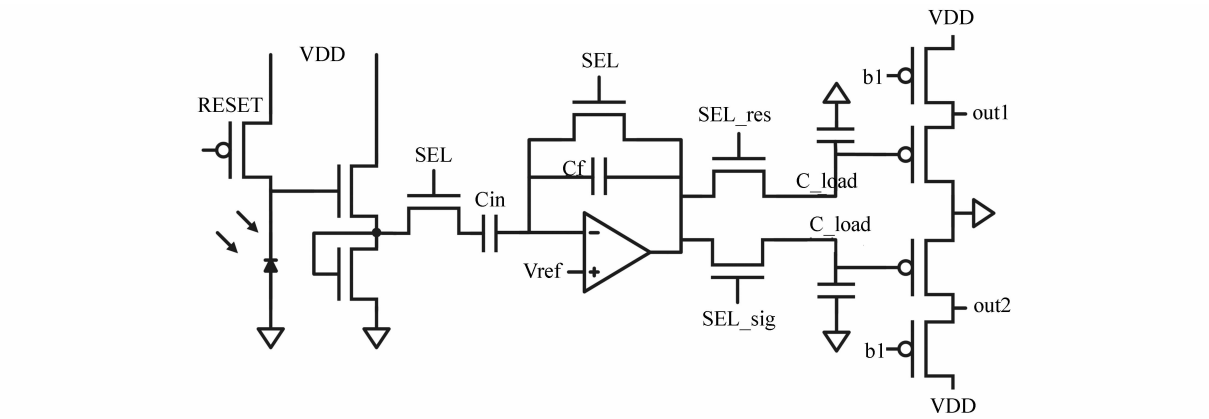

Fig. 4 Read-out circuit in CMOS sensor

图 4 CMOS 传感器读出电路

Pixel signal readout requires a column level circuit for further amplification and sampling output (shown in Fig. 4). The circuit mainly includes a CTIA (Capacitive Transimpedance Amplifier), an amplifier (for signal amplification), sample and hold circuits (for correlation double sampling) and source followers (for output drive).

4 Detector performance analysis

4.1 Differences in structure and process

The standard LV-CMOS process provides a PN photodiode structure based on a low resistivity P-substrate and an N-well. Both PMOS and NMOS are fabricated in wells (Twin-well process). Compared with the PIN photodiodes in the HV-CMOS process, the space charge region (depletion layer) of the two photosensitive elements is quite different (shown in Fig. 5), which introduces significant changes to the photo response characteristics of PIN and PN photodiodes.

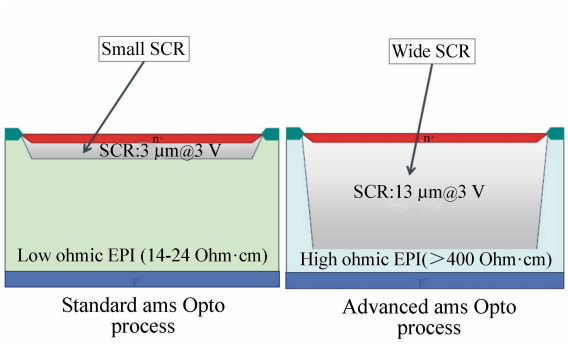

Fig. 5　Space charge regions of PN and PIN

图 5　PN 和 PIN 空间电荷区

Tab. 1　Formula parameters

表 1　公式参数

Parameter	PN photodiode (LV-CMOS)	PIN photodiode (HV-CMOS)
Area junction capacitance for zero bias: CJ	97 pF/mm^2	0.93 pF/mm^2
Area capacitance grading coefficient: MJ	0.31	0.05
Area capacitance junction potentials: PB	0.42 V	0.31 V
Perimeter junction capacitance for zero bias: CJSW	0.52 pF/mm	0.35 pF/mm
Perimeter capacitance grading coefficient: MJSW	0.21	0.21
Perimeter capacitance junction potentials: PBSW	0.38 V	0.16 V
Area leakage current density: JS	1.27 pA/mm^2	2.07 pA/mm^2
Perimeter leakage current density: JSSW	28.8 fA/mm	2.91 pA/mm
Voltage dependent area leakage conductivity: GLEAK	0 pA/V/mm^2	0 pA/V/mm^2
Voltage dependent perimeter leakage conductivity: GLEAKSW	44 fA/V/mm	1.29 pA/V/mm

4.2 Junction capacitance and dark current

Junction capacitance and dark current are two important characteristics of photodiodes, in which junction capacitance is related to charge conversion gain, while dark current mainly affects the dynamic range of the detector and introduces shot noise.

The junction capacitance and dark current of PN and PIN photodiodes in the standard LV-CMOS and HV-CMOS processes can be expressed in formulas (1) and (2), respectively.

$$C_{\mathrm{pd}} = \frac{W \cdot L \cdot CJ}{\left(1 - \frac{V}{PB}\right)^{MJ}} + \frac{2 \cdot (W + L) \cdot CJSW}{\left(1 - \frac{V}{PBSW}\right)^{MJSW}}, \tag{1}$$

$$I_{\mathrm{d}} = (JS + GLEAK \cdot V) \cdot WL + (JSSW + GLEAKSW \cdot V) \cdot 2 \cdot (W + L), \tag{2}$$

where W and L are the dimensions of a diode's cross section and V is the reverse bias voltage of the photodiode. At room temperature, the parameters of different processes are shown in Tab. 1.

To simplify the analysis, the photodiode's cross

section is set to a square such that $W = L$. Using formula 1, the relationship between junction capacitance and bias voltage (V) of different pixel sizes (L) (shown in Fig. 6) and between junction capacitance and pixel size (L) of different bias voltages (V) (shown in Fig. 7) can be obtained.

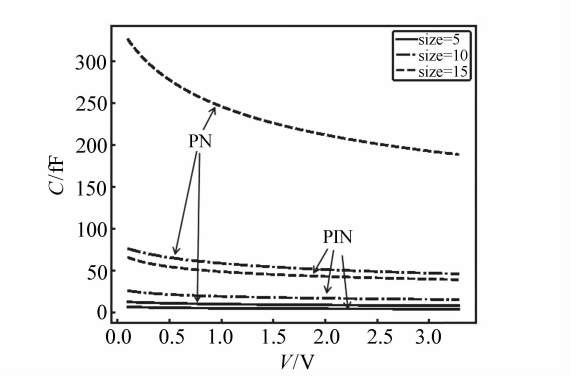

Fig. 6 Relationship between junction capacitance and bias voltage

图 6 结电容随偏压变化关系

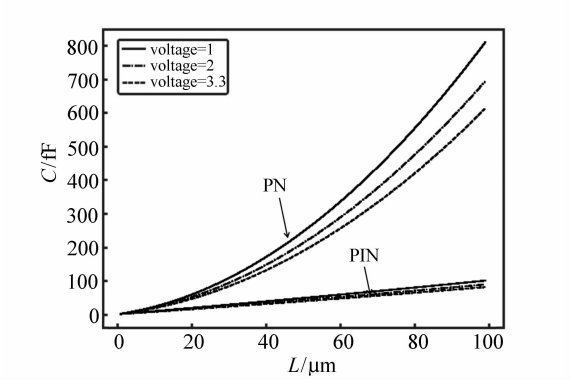

Fig. 7 Relationship between junction capacitance and pixel size

图 7 结电容与像素大小的关系

It can be seen that the junction capacitance of the PN photodiode is larger than that of the PIN photodiode with the same area and bias voltage. In large pixels ($L > 80$ μm), the junction capacitance of the PN photodiode is almost one order of magnitude larger than that of the PIN photodiode. Even in small pixels ($L \approx 20$ μm), the junction capacitance of the PN photodiode is also about 5 times of that of PIN photodiode. The junction capacitance of both of them varies obviously at low voltages (< 1 V) while it varies little when the voltage is higher than 2 V. As shown in Fig. 7, the junction capacitance of the PIN photodiode is linear with the length of the pixel, while the junction capacitance of PN photodiode is quadratic. This shows that the junction capacitance is mainly determined by the perimeter capacitance in the PIN photodiode, while the junction capacitance of the PN photodiode is mainly determined by the area capacitance. At the same time, the junction capacitance of the PIN is mainly determined by the perimeter capacitance, which indicates that the photosensitive element with small pixels also has a wide depletion region in the transverse direction. As a result, smaller photodiodes can achieve the same quantum efficiency as larger photosensitive surfaces.

Using formula 2, the relationship between dark current and bias voltage at different pixel sizes (L) (shown in Fig. 8), and the relationship between dark current and pixel size L at different bias voltages (shown in Fig. 9) can be obtained.

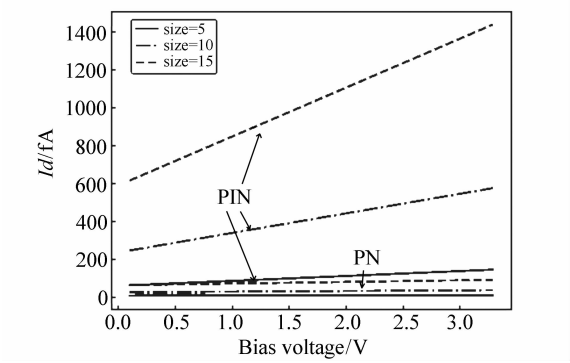

Fig. 8 Relationship between dark current and bias voltage

图 8 暗电流与偏置电压大小的关系

It can be seen that under the same area and bias voltage, the dark current of a PIN photodiode is larger than that of a PN photodiode, generally 1 – 2 orders of magnitude higher. Therefore, in applications, PIN photodiodes need to be cooled. As shown in Fig. 9, the dark current is linearly related to the length L, which indicates that the dark current is mainly composed of the perimeter leakage current.

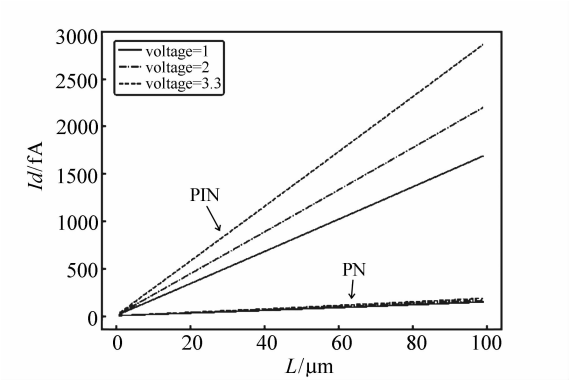

Fig. 9　Relationship between dark current and pixel size

图 9　暗电流与尺寸 L 的变化关系

4.3 Sensitivity of devices

Charge conversion gain CG is one of the most important characterization parameters of a detector's sensitivity, which reflects the effect of signal charge on junction voltage. Usually, the junction capacitance of a diode is considered as a planar capacitor. As a result, for a given signal charge ΔQ, the voltage variation ΔV on the junction capacitance C_{pd} satisfies the following relationship:

$$\Delta Q = C_{pd} \cdot \Delta V . \tag{3}$$

Therefore, the charge conversion gain CG equals to $1/C_{pd}$ [13].

For PIN photodiodes, the situation is more complicated. As analyzed earlier, the junction capacitance of a PIN photodiode varies with the bias voltage, especially at low bias voltages. This means that its junction capacitance is continuously changing during the integral process of the signal charge. It cannot be calculated using the method in formula (3). Instead, the numerical calculation method can be used.

The voltage variation ΔV caused by the charge is the difference between the reset voltage V_{reset} and the pixel voltage V_{pixel}. When the parasitic capacitance of the reset transistor and the follower transistor is ignored, the photodiode satisfies the charge formula at any time:

$$Q = V_{pd} \cdot C_{pd}. \tag{4}$$

The charge variation on the junction capacitor is the sum of the signal charge (Q_s) and the dark current charge (Q_d) from the start of reset to the integration time t_i. That is,

$$Q_s + Q_d = (I_s + I_d) \cdot t_i , \tag{5}$$

therefore,

$$V_{reset} \cdot C_{Pd0} - V_{Pd} \cdot C_{Pd} = (I_s + I_d) \cdot t_i , \tag{6}$$

where C_{pd0} is the junction capacitance of the PIN photodiode at the initial time, I_s is the photo current, and I_d is the dark current. Accordingly,

$$V_{pd} \cdot C_{pd} = V_{reset} \cdot C_{Pd0} - (I_s + I_d) \cdot t_i . \tag{7}$$

Therefore, given the pixel size, fixed reset voltage V_{reset} and integration time t_i, the relationship curve between the junction voltage V_{pd} and the photo current I_s can be obtained by numerical calculation (shown in Fig. 10).

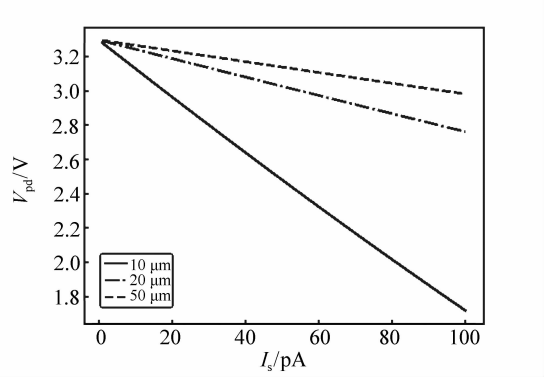

Fig. 10　Relationship between junction voltage and photo current

图 10　结电压与光电流关系

Fig. 10 shows the variation of junction voltage with photo-current for different PIN photodiode sizes when the reset voltage is 3.3 V and the integration time is 100 μs. It must be noted that the variation of junction voltage includes the influence of dark current, and the influence of dark current need to be removed in order to obtain the variation of voltage caused by signal charge.

The voltage variation caused by the dark current is equal to the voltage variation when light is absent. That is:

$$\Delta V_d = V_{reset} - V_{pd}(I_s = 0) . \tag{8}$$

Therefore, the voltage change caused by the photo signal is:

$$\Delta V_s = V_{reset} - V_{pd} - \Delta V_d. \quad (9)$$

Using the above formula, under the same conditions as in Fig. 10, the relationship between voltage variation and photocurrent (shown in Fig. 11) can be obtained, which essentially varies linearly.

Therefore the average charge gain CG in an integral time t_i can be expressed as:

$$CG = \frac{\Delta V_s}{I_s \cdot t_i}. \quad (10)$$

This reflects the average sensitivity of the integral charges, which is closely related to junction capacitance. Usually, small signal sensitivity needs to be considered. Specifically, that is the instantaneous charge gain of pixels CG':

$$1/CG' = \frac{\partial Q}{\partial V} = \frac{\partial (C_{pd} \cdot V)}{\partial V} = C_{pd} + V\frac{\partial C_{pd}}{\partial V} = C_{pd}\left(1 + \frac{V}{C_{pd}}\frac{\partial C_{pd}}{\partial V}\right). \quad (11)$$

Since the junction capacitance of the PIN photodiode decreases with an increase of voltage (*i. e.*, $\partial C_{pd}/\partial V$ is a negative value) the transient charge gain of the pixel is higher than the reciprocal of the transient capacitance $1/C_{pd}$, which is usually considered as charge gain.

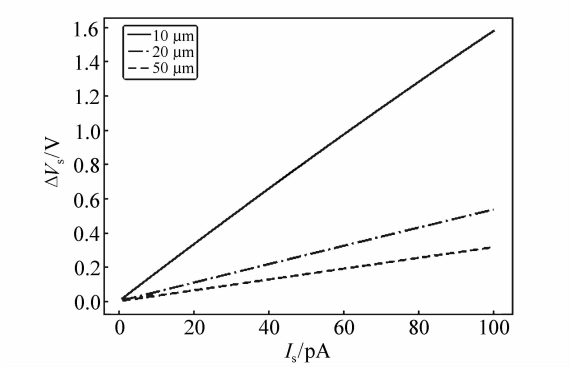

Fig. 11 Relationship between photo signal voltage variation and photo current

图 11 光信号电压变化与光电流关系

In Fig. 11, although the independent variable is photo current I_s, since the integration time t_i is fixed, the independent variable can be considered as signal charge. By deriving the curve, the transient charge gain curve in the process of self-integration (shown in Fig. 12) is obtainable.

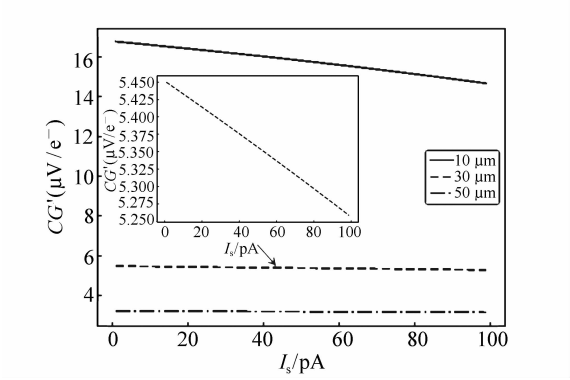

Fig. 12 Relationship between transient charge conversion gain and photo current variance

图 12 瞬态电荷转换增益随光电流变化关系

It can be seen from the graph that small pixels have a higher charge gain and that a small signal gain gradually decreases with the increase in photocurrent. This is more obvious with the small pixel. Therefore, in order to obtain higher pixel charge gain in low-light detection, smaller pixels should be selected.

Finally, we calculate the instantaneous junction capacitance of the pixel in the integration process and compare its reciprocal ($1/C_{pd}$) with the real instantaneous charge gain (shown in Fig. 13). Here, the pixel size is 10 μm × 10 μm.

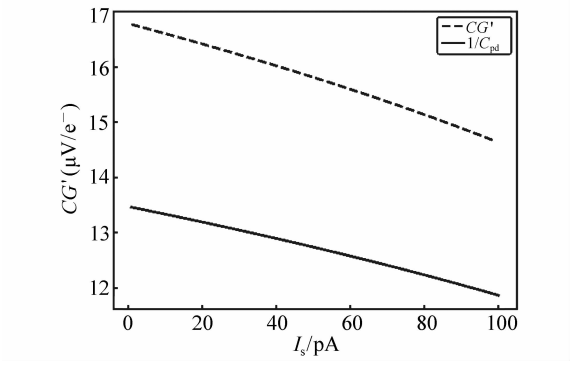

Fig. 13 Comparison between transient charge gain and the reciprocal of capacitance value

图 13 瞬态电荷增益与电容值倒数的比较

It can be seen that the transient charge gain of

pixels is always greater than the reciprocal of junction capacitance, which is consistent with the analysis of Eq. 11. Under 10 μm × 10 μm pixel size, the instantaneous charge gain reaches 16 μV/e⁻. By using PIN photodiodes, we can not only obtain higher average charge gain (their capacitance is smaller than that of PN photodiodes) but also obtain higher transient charge gain than conventional methods. The transient charge gain of the pixel is the same as quantum efficiency, which reflects the charge sensitivity of the photosensitive element.

4.4 Noise analysis of devices

The equivalent input noise of the CMOS image sensor can be expressed as the sum of noise produced by pixel and noise produced by readout circuit:

$$n_{n,\text{input}}^2 = n_{n,\text{pix}}^2 + \frac{v_{n,\text{circuit}}^2}{(A_{\text{tot}} \cdot G_e)^2}, \quad (12)$$

where $n_{n,\text{pix}}$ is the number of noise electrons produced by PIN photodiodes, $v_{n,\text{circuit}}$ is the equivalent output noise voltage of the on-chip readout circuit, A_{tot} is the total voltage gain of the on-chip circuit, and G_e is the charge conversion gain of the PIN photodiode. Here $G_e = q \cdot CG$, where q is the charge of electrons.

4.4.1 Noise of the PIN photodiode

The noise of the PIN photodiode mainly includes shot noise and reset (kTC) noise. Since the reset noise can be suppressed by correlated double sampling, the dominant one is shot noise. Shot noise is caused by the discreteness of the carriers that form the current, and is usually regarded as white noise. In PIN, shot noise is related to dark current and incident photon. The electron number of shot noise can be expressed as[14]:

$$n_{\text{n,pix}}^2 = N_{\text{dark}} + N_{\text{sig}}. \quad (13)$$

In a certain integration time t_i, the dark current noise electrons N_{dark} and photo-generated noise electrons N_{sig} can be expressed as

$$N_{\text{dark}} = \frac{Q_{\text{dark}}}{q} = \frac{I_d \cdot t_i}{q}. \quad (14)$$

$$N_{\text{sig}} = \frac{Q_s}{q} = \frac{I_s \cdot t_i}{q}. \quad (15)$$

The photocurrent of a PIN photodiode can be expressed as the product of the current responsivity R_i) and the incident light power(P), *i.e.*,

$$I_s = R_i \cdot P, \quad (16)$$

and the incident light power(P) can be expressed as the product of the light power per unit area(E_v) and the area of the photosensitive surface (l^2, l is the length of the photosensitive surface):

$$P = l^2 \cdot E_v.$$

Therefore, photocurrent can also be expressed as:

$$I_s = R_i \cdot l^2 \cdot E_v. \quad (17)$$

4.4.2 The noise of the readout circuit

The readout circuit of a CMOS image sensor mainly includes a source follower, a CTIA amplifier and a sample and hold circuit.

The source follower is used to drive the output of the signal. It is used in two parts of the circuit, which are used for pixel signal readout and final output drive. The CTIA is the core part of the CMOS image sensor readout circuit, which mainly includes a single-ended cascode amplifier and a feedback loop composed of two capacitors, as shown in Fig. 14.

The total gain A_{tot} of the CMOS image sensor readout circuit is the product of the gain of the above three parts, which is a fixed value before saturation. At the same time, the equivalent output noise voltage of the on-chip readout circuit can also be regarded as a constant at a given bandwidth[15]. In this paper, readout circuits are designed by the 0.35 μm HV-CMOS process.

4.5 Analysis of low light level detection capability of devices

Noise equivalent power (NEP) is the incident light power(P_1) when the signal and noise are equal ($SNR = 1$) in the detector, $NEP = P_1$. According to the definition, the smaller the value, the better the detector performance.

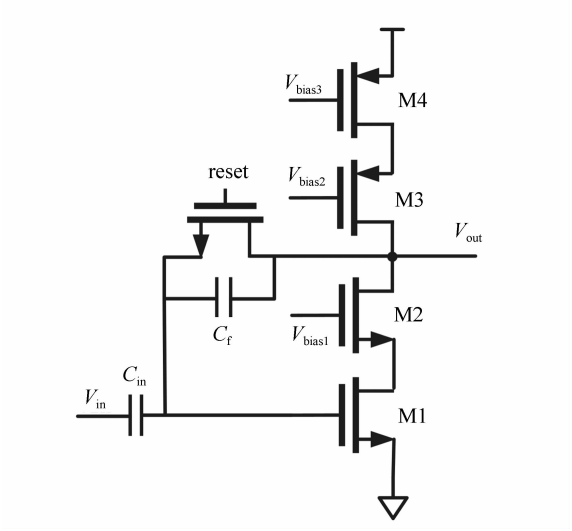

Fig. 14 Schematic diagram of a CTIA structure

图 14 CTIA 结构示意图

When the signal-to-noise ratio(SNR) equals 1, $N_{sig} = n_{n,input}$, where $n_{n,input}$ is the total equivalent input noise. Bringing the relevant formula to it,

$$\left(\frac{Rl^2 t_i}{q}\right)^2 E_v^2 = \frac{Rl^2 t_i}{q} E_v + \frac{v_{n,circuit}^2}{(A_{tot} \cdot G_e)^2} + \frac{I_d t_i}{q}. \tag{18}$$

For convenience of calculation, the above formula can be rewritten as:

$$a_0^2 E_v^2 = a_0 E_v + a_1, \tag{19}$$

then, the solution can be obtained:

$$E_v = \frac{1 + \sqrt{(1 + 4a_1)}}{2a_0}, \tag{20}$$

therefore,

$$NEP = P_1 = l^2 E_v. \tag{21}$$

Combined with $a_0 = (R_i l^2 t_i)/q$, it can be concluded that l^2/a_0 is a quantity independent of pixel size. Meanwhile, from the above analysis, we know that as l increases, G_e decreases and I_d increases. a_1 also increases with l. So, the relationship between the *NEP* and the pixel size for integration times less than 100 μs, a 3.3 V reset voltage and 0.5 A/W current responsivity (shown in Fig. 15) can be obtained. The results show that, for the detector integrated with a PIN photosensitive element and a CMOS circuit developed by the HV-CMOS process, when the pixel is 20 μm × 20 μm, the device's NEP can reach 0.08 pW in a short integration time(100 μs). This result is nearly 2 times lower than that of the detector of the same size developed by the standard LV-CMOS process.

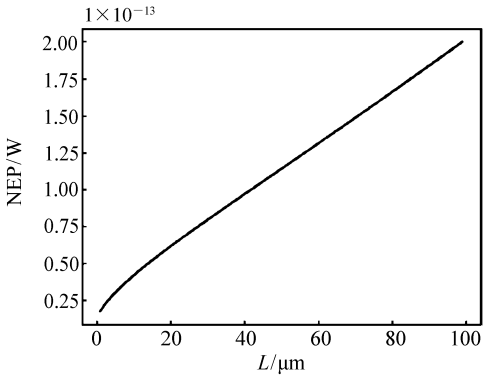

Fig. 15 Relationship between NEP and pixel size

图 15 NEP 与像素大小的关系

5 Conclusions

In this paper, a CMOS image sensor with 3T pixel structure integrated with PIN photosensitive elements was analyzed theoretically and the relationship between photo-response characteristics and noise equivalent power and the pixel size and bias voltage were studied in depth. The results show that generally, the junction capacitance of a PIN diode is about one order of magnitude lower than that of a PN diode, meaning that the PIN photodiode has higher charge conversion gain. Meanwhile, its transient charge gain is higher than $1/C_{pd}$. Therefore, the equivalent input noise of a detector integrated with PIN photosensitive elements should be one order of magnitude lower under the same readout circuit. Because smaller pixels have smaller junction capacitance and dark current, they also have smaller NEP. This research should be instructive for the design of low-light level detectors.

——中文对照版——

1　引　言

微光成像是指在低照度(照度 $< 10^{-2}$ lx)环境中的光学成像过程。在航空航天、气象观测以及军事侦查等领域,微光成像技术都发挥着极为重要的作用[1-4]。随着 CMOS 工艺的发展,CMOS 图像传感器开始替代 CCD,逐步向微光成像领域扩展[5-7]。目前,由于 CMOS 工艺兼容性的限制,最为常用的 CMOS 图像传感器一般采用 3T 或 4T 像素结构,并且光电二极管均是以 PN 型为基本构成。4T 像素由于增加了电荷转移管和读出浮置电容,可以实现更高的灵敏度和更低的噪声,但同时也限制了像素的大小,不适合大像素器件的研制。PIN 光电二极管是 PN 结光电二极管的特殊形式,具有结电容小、响应速度快、量子效率高等优点[8],对像素大小也没有绝对的限制。但 PIN 光敏元的制作与标准低压 CMOS 工艺(LV-CMOS)不兼容。目前,对 PIN 光敏元与 CMOS 电路集成的研究大多基于 SOI 工艺[9-10]。

在本文中,将对采用 HV-CMOS 工艺的以 PIN 光电二极管为光敏元的 CMOS 图像传感器的光电响应特性进行分析,重点研究像素尺寸与复位电压对探测器光电响应特性和噪声等效功率(NEP)的影响。

2　HV-CMOS 工艺

与标准 LV-CMOS 工艺相比,HV-CMOS 工艺(图 1)在重掺杂的 p 型衬底之上增加一层厚度约为 20 μm 的轻掺杂 p 型外延层,电阻率为 400 ~ 1 000 Ω · cm。同时,为了实现 CMOS 电路对衬底低电阻率(1 ~ 10 Ω · cm)的要求,该工艺在制作 PMOS 和 NMOS 之前,首先 MOS 管区域的高阻 P 型外延层上制备深阱 N 层,MOS 在深阱 N 层上再按照标准 LV-CMOS 工艺制备,而光敏元则直接在高阻的 P 型外延层上制备,形成 PIN 光敏元与 CMOS 电路的单片集成(图 2)[11]。

采用这种工艺制备的 CMOS 电路具有高压工作的能力,目前已是标准 CMOS 工艺的一种。

本工艺中,PIN 光电二极管由重掺杂的 p(p +)型区域(P 层)、轻掺杂的 p(p -)型外延层(I 层)以及重掺杂的 n(n +)型区域(N 层)组成。其本征层(I 层)的存在,增加了耗尽区的宽度,提高了二极管的光电量子效率,这是 PIN 光电二极管灵敏度高于 PN 结光电二极管的根本原因所在。另一方面,本工艺还可以去除 PIN 光敏元表面在 CMOS 工艺过程中形成的很厚的介质层,代之以单层抗反射介质,使得光敏元的量子效率得到进一步提高。

3　3T 像素结构

以 PIN 为光敏元的 CMOS 传感器可以采用 3T 像素结构(图 3)。该结构具有结构简单、填充系数高等优点[12]。在像素结构中,PIN 光电二极管是整个 CMOS 图像传感器中唯一感光的部分;M1 是复位管,当信号被读出后,光电二极管通过复位管复位至反偏电压值;M2 是跟随管,负责像素信号的读出。为了减小电荷注入效应的影响,复位管的尺寸应当尽可能的小。

相比于 3T 像素结构,4T 像素在光电二极管后面增加了电荷转移管和需要特殊设计的浮置电容,从而能够实现真正的相关双采样,但这也使得 4T 像素工艺复杂、成本较高。同时,为实现更高的灵敏度,浮置电容容值较小,从而不利于大像素器件的研制。

像元信号读出需要列级电路进行进一步放大和采样输出(图 4)。列级电路主要包括 CTIA 放大器(用于信号放大)、采样保持电路(用于相关双采样)和源极跟随器。

4　探测器性能分析

4.1　结构和工艺差异

标准 LV-CMOS 工艺提供了基于低阻 P 型衬底与 N 阱的 PN 结光电二极管结构,片上电路中的 PMOS 和 NMOS 都制作在阱中(双阱工艺)。

与 HV-CMOS 工艺中的 PIN 光电二极管相比，两种光敏元的空间电荷区（耗尽层）存在较大的差异（图 5），这使得 PIN 和 PN 光电二极管在光电响应特性上发生了极大的变化。

4.2 结电容和暗电流

结电容和暗电流是光电二极管两个极为重要的特性，其中，结电容与电荷转换增益有关，而暗电流则主要影响探测器的动态范围，并引入散粒噪声。

标准 LV-CMOS 和 HV-CMOS 工艺下，PN 和 PIN 光电二极管的结电容和暗电流都分别可以用式（1）和式（2）表示：

$$C_{\mathrm{pd}} = \frac{W \cdot L \cdot CJ}{\left(1 - \frac{V}{PB}\right)^{MJ}} + \frac{2 \cdot (W + L) \cdot CJSW}{\left(1 - \frac{V}{PBSW}\right)^{MJSW}}, \tag{1}$$

$$I_{\mathrm{d}} = (JS + GLEAK \cdot V) \cdot WL + (JSSW + GLEAKSW \cdot V) \cdot 2 \cdot (W + L), \tag{2}$$

其中，W 和 L 分别是二极管的尺寸，V 是光电二极管的反偏电压。室温下，不同工艺下的各参数值如表 1 所示。

为了简化分析，选取光电二极管的横截面为一正方形，即 $W = L$。通过公式（1），可以得出不同像素尺寸（L）下结电容与偏压（V）的关系（图 6）以及不同偏压（V）下结电容与像素尺寸（L）的关系（图 7）。

可以看出，在相同面积、相同偏压下，PN 结电容要明显大于 PIN 结电容；在大像素（$L > 80$ μm）中，PN 结电容差不多要比 PIN 大一个数量级，即使在小像素（$L \approx 20$ μm）下，PN 结电容也要接近 PIN 结电容的 5 倍左右。其中，低压下（<1 V）结电容变化较为明显，而当电压 >2 V 时，两者结电容都变化不大。在图 7 中还可以看出，PIN 结电容与像素边长基本呈线性关系，而 PN 结电容则与边长 L 呈二次方关系，这表明，在 PIN 二极管中，结电容主要是由边长电容决定的；而 PN 结电容则主要是面积电容。同时，小像素情况下 PIN 光敏元的结电容主要由边长电容决定，说明光敏元在横向也存在较宽的耗尽区。这一特性意味着较小的光电二极管设计事实上可以实现与较大光敏面相同的光电量子效率。

利用公式（2）可以得到不同像素尺寸（L）下暗电流与偏压的关系（图 8）以及不同偏压下暗电流与尺寸 L 的关系（图 9）。

可以看出，相同面积和偏压下，PIN 光电二极管的暗电流要比 PN 光电二极管高 1 ~ 2 个数量级，因此，在应用中，PIN 光电二极管需要进行降温。在图 9 中，还可以得到，两者的暗电流与边长 L 都呈线性关系，这表明，暗电流主要由边缘漏电流组成。

4.3 器件的灵敏度

电荷转换增益 CG 反映了信号电荷对结电压的影响情况，是探测器灵敏度的重要表征参数之一。通常情况下，将二极管的结电容看作为一平板电容器，因此，对于一定的信号电荷 ΔQ，其在结电容 C_{pd} 上所引起的电压变化量 ΔV 满足如下关系：

$$\Delta Q = C_{\mathrm{pd}} \cdot \Delta V. \tag{3}$$

因此，其电荷转换增益 CG 就等于 $1/C_{\mathrm{pd}}$[13]。

而对于 PIN 光电二极管来讲，情况则稍显复杂。正如前面所分析的那样，PIN 的结电容随偏置电压变化而变化，在低偏压下，情况更加明显。这就意味着信号电荷在自积分过程中，其结电容也在随之改变着。显然，无法像式（3）那样进行计算，在此可以采用数值计算的方法。

对于电荷造成的电压变化 ΔV，它是复位电压 V_{reset} 与积分后电压 V_{pixel} 的差值。在忽略复位管和跟随管寄生电容的情况下，在任何一个时刻，光电二极管都满足电荷公式：

$$Q = V_{\mathrm{pd}} \cdot C_{\mathrm{pd}}. \tag{4}$$

从复位开始到积分 t_{i} 时间后，结电容上的电荷变化为信号电荷（Q_{s}）与暗电流电荷（Q_{d}）之和，即：

$$Q_{\mathrm{s}} + Q_{\mathrm{d}} = (I_{\mathrm{s}} + I_{\mathrm{d}}) \cdot t_{\mathrm{i}}, \tag{5}$$

因此：

$$V_{\mathrm{reset}} \cdot C_{\mathrm{Pd0}} - V_{\mathrm{Pd}} \cdot C_{\mathrm{Pd}} = (I_{\mathrm{s}} + I_{\mathrm{d}}) \cdot t_{\mathrm{i}}, \tag{6}$$

其中，C_{pd0} 是 PIN 光电二极管初始时刻的结电容值，I_{s} 是光电流，I_{d} 是暗电流。经整理可得：

$$V_{\mathrm{pd}} \cdot C_{\mathrm{pd}} = V_{\mathrm{reset}} \cdot C_{\mathrm{Pd0}} - (I_{\mathrm{s}} + I_{\mathrm{d}}) \cdot t_{\mathrm{i}}. \tag{7}$$

因此，在给定像素尺寸以及固定复位电压 V_{reset} 和积分时间 t_{i} 的情况下，可以通过数值计算的方法得到积分后结电压 V_{pd} 与光电流 I_{s} 的关系曲线（图 10）。

图 10 为在复位电压为 3.3 V、积分时间为 100 μs 下,不同尺寸 PIN 光电二极管积分后结电压随光电流的变化关系。必须注意到,结电压的变化包含了暗电流的影响,因此,为了获得由信号电荷而带来的电压变化量,需要将暗电流的影响去除。

暗电流造成的电压变化就等于在无光情况下的电压变化,即

$$\Delta V_{\mathrm{d}} = V_{\mathrm{reset}} - V_{\mathrm{pd}}(I_{\mathrm{s}} = 0), \tag{8}$$

因此,光电信号电压变化量 ΔV_{s} 为

$$\Delta V_{\mathrm{s}} = V_{\mathrm{reset}} - V_{\mathrm{pd}} - \Delta V_{\mathrm{d}}. \tag{9}$$

使用上面的公式,在与图 10 相同的条件下,可以得到 ΔV_{s} 与光电流 I_{s} 之间的关系(图 11),两者基本呈线性变化。

因此,对于在一个积分时间 t_{i} 内的平均电荷增益 CG,可以表示为:

$$CG = \frac{\Delta V_{\mathrm{s}}}{I_{\mathrm{s}} \cdot t_{\mathrm{i}}}. \tag{10}$$

这反映了积分电荷的平均灵敏度,这与结电容密切相关。通常,还需要考虑小信号灵敏度,也就是像素的瞬态电荷增益 CG':

$$1/CG' = \frac{\partial Q}{\partial V} = \frac{\partial (C_{\mathrm{pd}} \cdot V)}{\partial V} = C_{\mathrm{pd}} + V\frac{\partial C_{\mathrm{pd}}}{\partial V} = C_{\mathrm{pd}}\left(1 + \frac{V}{C_{\mathrm{pd}}}\frac{\partial C_{\mathrm{pd}}}{\partial V}\right). \tag{11}$$

由于 PIN 光电二极管的结电容随电压增大而减小,即 $\partial C_{\mathrm{pd}}/\partial V$ 为一负值,因此,像素的瞬态电荷增益要高于通常认为的瞬态电容的倒数,即 $CG' > 1/C_{\mathrm{pd}}$。

考虑图 11,虽其自变量是光电流 I_{s},但由于积分时间 t_{i} 是固定的,可以将自变量看作是电荷量。对图中曲线求导,就可以得到自积分过程中瞬态电荷增益变化曲线(图 12)。

从图中可以看出,小像素拥有着更高的电荷增益;随着光电流的增大,小信号增益在逐渐减小,这在小像素尺寸中变化的更加明显。因此,在微光探测中,为了获得更高的像素电荷增益,应当选取较小的像素。

最后,计算像素在积分过程中的瞬态结电容值,并取其倒数($1/C_{\mathrm{pd}}$),也是通常认为的电荷增益,将其与真实的瞬态电荷增益作对比(图 13)。在此,选取的是 10 μm × 10 μm 的像素。

从图中可以看出,像素的瞬态电荷增益总是大于结电容的倒数,这与式(11)的分析相符。在 10 μm × 10 μm 像素大小下,像素的 CG 达到了 16 μV/e$^-$。通过使用 PIN 光电二极管,不仅可以获得更高的平均电荷增益(其结电容相比于 PN 光电二极管更小),还可以获得高于传统方法的瞬态电荷增益。而像素的瞬态电荷增益与量子效率一样,反映的是光敏元在小信号情况下的电荷灵敏度。

4.4　器件的噪声分析

CMOS 图像传感器的等效输入噪声可以表示为像素产生的噪声与外围电路产生的噪声之和,即:

$$n^2_{n,\mathrm{input}} = n^2_{n,\mathrm{pix}} + \frac{v^2_{n,\mathrm{circuit}}}{(A_{\mathrm{tot}} \cdot G_{\mathrm{e}})^2}, \tag{12}$$

在此,使用的是等效噪声电子数。其中,$n_{n,\mathrm{pix}}$ 是 PIN 光电二极管产生的噪声,$v_{n,\mathrm{circuit}}$ 是片上读出电路的等效输出噪声电压。A_{tot} 是片上电路总的电压增益,G_{e} 是 PIN 光电二极管的电荷转换增益。需要注意的是,G_{e} 与式(10)略有不同,由于需要得到的是噪声电子数,因此,可以认为 $G_{\mathrm{e}} = q \cdot CG$,其中 q 为电子的电荷量。

4.4.1　PIN 噪声

PIN 光电二极管的噪声主要包括散粒噪声以及复位(kTC)噪声。其中,由于复位噪声可以通过相关双采样进行抑制,因此占据主导地位的是散粒噪声。散粒噪声是由形成电流的载流子的离散性造成的,通常被认为是白噪声。在 CMOS 图像传感器中,散粒噪声由暗电流和入射光子有关。散粒噪声电子数可以被表示为[14]:

$$n^2_{\mathrm{n,pix}} = N_{\mathrm{dark}} + N_{\mathrm{sig}}, \tag{13}$$

其中,在一定积分时间 t_{i} 中,暗电流电荷 N_{dark} 和光生电荷 N_{sig} 分别可以表示为:

$$N_{\mathrm{dark}} = \frac{Q_{\mathrm{dark}}}{q} = \frac{I_{\mathrm{d}} \cdot t_{\mathrm{i}}}{q}, \tag{14}$$

$$N_{\mathrm{sig}} = \frac{Q_{\mathrm{s}}}{q} = \frac{I_{\mathrm{s}} \cdot t_{\mathrm{i}}}{q}. \tag{15}$$

PIN 光电二极管的光电流可以表示为电流响应度(R_{i})与入射光功率(P)的乘积,即

$$I_{\mathrm{s}} = R_{\mathrm{i}} \cdot P, \tag{16}$$

入射光功率(P)可以表示为单位面积光功率(E_{v})与感光面面积(l^2,l 是感光面长度)的乘积,即

$$P = l^2 \cdot E_v.$$

因此,光电流也可以表示为

$$I_s = R_i \cdot l^2 \cdot E_v. \tag{17}$$

4.4.2 读出电路噪声

CMOS 图像传感器的读出电路主要包括源极跟随器、电容跨阻放大器(CTIA)以及采样保持器。

源极跟随器主要是对输出信号进行驱动,电路中有两处使用到了源极跟随器,分别是用于像素信号读出和最终的输出驱动。

CTIA 是 CMOS 图像传感器读出电路的核心部分,结构主要包括:单端级联放大器以及两个电容组成的反馈回路,结构如图 14 所示。

CMOS 图像传感器读出电路的增益 A_{tot} 为上面 3 部分增益的乘积,在达到饱和前,这是一个定值。同时,在给定带宽下,片上读出电路的等效噪声也可以看成是常数[15]。在本文中,读出电路使用 0.35 μm 的 HV-CMOS 工艺进行设计。

4.4.3 器件的微光探测能力分析

噪声等效功率(NEP)是指光电探测器中信号和噪声相等时($SNR = 1$)的入射光功率(P_1),即 $NEP = P_1$。根据定义,该值越小表示探测器性能越好。

当信噪比等于 1 时,得到 $N_{sig} = n_{n,input}$,将相关公式带入可得:

$$\left(\frac{Rl^2 t_i}{q}\right)^2 E_v^2 = \frac{Rl^2 t_i}{q} E_v + \frac{v_{n,circuit}^2}{(A_{tot} \cdot G_e)^2} + \frac{I_d t_i}{q}. \tag{18}$$

为了方便计算,将上式改写为

$$a_0^2 E_v^2 = a_0 E_v + a_1, \tag{19}$$

可以求得:

$$E_v = \frac{1 + \sqrt{(1 + 4a_1)}}{2a_0}. \tag{20}$$

因此,信噪比等于 1 时的入射光功率 P_1(NEP)为

$$NEP = P_1 = l^2 E_v. \tag{21}$$

结合 $a_0 = (Rl^2 t_i)/q$,可以得出 l^2/a_0 是一个与像素大小无关的量,而在上面分析中,已知:l 增大,G_e 减小,I_d 增大,因此,a_1 也会随 l 增大而增大。可以得到,在积分时间 100 μs、复位电压为 3.3 V 以及响应度为 0.5 A/W 的条件下,器件的 NEP 与像素大小的关系如图 15 所示。从该结果可以得知,对于采用 HV-CMOS 工艺研制的 PIN 光敏元与 CMOS 电路单片集成的探测器,当像素在 20 μm × 20 μm 时,在短积分时间(100 μs)的情况下,器件的 NEP 可以达到 0.08 pW。这一结果比相同大小的标准 LV-CMOS 探测器低了近 2 倍。

5 结 论

本文对集成了 PIN 光敏元的 3T 像素 CMOS 图像传感器进行了理论分析,重点研究了光电响应特性和噪声等效功率与像素大小以及偏置电压的关系。研究表明,在其他条件都相同的情况下,PIN 二极管的结电容比 PN 结二极管要低一个数量级左右,因此,PIN 也拥有了更高的电荷转换增益;同时,PIN 的瞬态电荷增益要高于通常认为的 $1/C_{pd}$。所以,在外围电路相同的情况下,集成了 PIN 光敏元的探测器的等效输入噪声也要低一个数量级;同时,由于小像素的结电容和暗电流更小,因此也就拥有了更小的 NEP。该研究结果对微光探测器设计具有指导意义。

参考文献:

[1] 何家维,何昕,魏仲慧,等. 高灵敏度 EMCCD 导航相机的设计[J]. 光学 精密工程,2018,26(12):3019-3027.
HE J W,HE X,WEI ZH H,*et al*.. Design of high-sensitivity EMCCD navigation camera[J]. *Opt. Precision Eng.*,2018,26(12):3019-3027. (in Chinese)

[2] 何伟基,司马博羽,程耀进,等. 基于盖格-雪崩光电二极管的光子计数成像[J]. 光学 精密工程,2012,20(8):1831-1837.
HE W J,SIMA B Y,CHENG Y J,*et al*.. Photon counting imaging based on GM-APD[J]. *Opt. Precision Eng.*,2012, 20(8):1831-1837. (in Chinese)

[3] 刘超,张晓晖. 超低照度下微光图像的深度卷积自编码网络复原[J]. 光学 精密工程,2018,26(4):951-961.

LIU CH, ZHANG X H. Deep convolutional autoencoder networks approach to low-light level image restoration under extreme low-light illumination[J]. *Opt. Precision Eng.*, 2018, 26(4): 951-961. (in Chinese)

[4] 陈莹, 朱明, 刘剑, 等. 高斯混合模型自适应微光图像增强[J]. 液晶与显示, 2015, 30(2): 300-309.
CHEN Y, ZHU M, LIU J, *et al.*. Automatic low light level image enhancement using Gaussian mixture modeling[J]. *Chinese Journal of Liquid Crystals and Displays*, 2015, 30(2): 300-309. (in Chinese)

[5] 王田珲, 李豫东, 文林, 等. CMOS 图像传感器在质子辐照下热像素的产生和变化规律[J]. 发光学报, 2018, 39(12): 1697-1704.
WANG T H, LI Y D, WEN L, *et al.*. Generation and annealing of hot pixels of CMOS image sensor induced by proton[J]. *Chinese Journal of Luminescence*, 2018, 39(12): 1697-1704. (in Chinese)

[6] 玛丽娅, 李豫东, 郭旗, 等. CMOS 有源像素图像传感器的电子辐照损伤效应研究[J]. 发光学报, 2017, 38(2): 182-187.
MA L Y, LI Y D, GUO Q, *et al.*. Electron beam radiation effects on CMOS active pixel sensor[J]. *Chinese Journal of Luminescence*, 2017, 38(2): 182-187. (in Chinese)

[7] 徐守龙, 邹树梁, 黄有骏, 等. CCD 与 CMOS 像素传感器 γ 射线电离辐射响应特性对比研究[J]. 发光学报, 2018, 39(6): 815-822.
XU SH L, ZOU SH L, HUANG Y J, *et al.*. Comparative study on γ-ray radiation response characteristics of CCD and CMOS pixel sensor[J]. *Chinese Journal of Luminescence*, 2018, 39(6): 815-822. (in Chinese)

[8] 施敏, 伍国珏. 半导体器件物理[M]. 耿莉, 张瑞智, 译. 西安: 西安交通大学出版社, 2008.
SHI M, WU G Y. *Physics of Semiconductor*[M]. GENG L, ZHANG R ZH, trans. Xi'an: Xi'an JiaoTong University Press, 2008. (in Chinese)

[9] MARUYAMA T, MAEKITA K, LI G, *et al.*. High speed operation of SOI PIN photodiodes fabricated by CMOS compatible process[C]. Proceedings of 2014 OptoElectronics and Communication Conference and Australian Conference on Optical Fibre Technology, IEEE, 2014.

[10] MITSUNO H, MARUYAMA T, IIYAMA K, *et al.*. Sub-μm electrode spacing SOI-PIN photodiode fabricated by CMOS compatible process[C]. Proceedings of the 21st Opto, Electronics and Communications Conference (OECC) held jointly with 2016 International Conference on Photonics in Switching, IEEE, 2016.

[11] JONAK-AUER I, TEVA J, PARK J M, *et al.*. New integration concept of PIN photodiodes in 0.35 μm CMOS technologies[J]. *Proceedings of SPIE*, 2012, 8431: 843115.

[12] BIGAS M, CABRUJA E, FOREST J, *et al.*. Review of CMOS image sensors[J]. *Microelectronics Journal*, 2006, 37(5): 433-451.

[13] NAKAMURA J. *Image Sensors and Signal Processing for Digital Still Cameras*[M]. Boca Raton: CRC Press, 2006.

[14] OHTA J. *Smart CMOS Image Sensors and Applications*[M]. Boca Raton: CRC Press, 2008.

[15] RAZAVI B. *Design of Analog CMOS Integrated Circuit*[M]. 2nd ed. New York: McGraw-Hill Education, 2017.

Author biographies:

YANG Cheng-cai (1992—): Tai′ An, Shandong Province, Graduated from Northeastern University in 2016, and currently pursuing a master′s degree in Shanghai Institute of Technical Physics, Chinese Academy of Sciences. He mainly engages in the research of CMOS image sensor design and read-out circuits design. E-mail: tomasyoung@mail.ustc.edu.cn.

CHEN Yong-ping (1963—): Professor, Shanghai Institute of Technical Physics, Chinese Academy of Sciences. His research interests are on design of high-performance CMOS image sensors. E-mail: chen_yp@mail.sitp.ac.cn